AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A semiconductor ~~device comprising a non-volatile memory, said non-volatile~~ memory, ~~including~~ comprising:

a memory cell array constituted by memory cells, each memory cell ~~which have~~ having a floating electrode[[s]], ~~and are~~ the memory cells being arranged in ~~the shape of~~ a matrix on a semiconductor substrate;

~~element isolating regions, each of which has~~ a plurality of first trenches formed in said semiconductor substrate, [[and]] each first trench being formed between said memory cells adjacent to each other along a gate width direction[[,]]; ~~and an~~

a plurality of isolating fillers filled in said first trenches;

a plurality of second trenches formed in said isolating fillers, each said second trench being formed [[and]] between said floating electrodes of adjacent ones of said memory cells ~~adjacent to each other~~ along the gate width direction ~~and~~, a maximum width of said second trenches being ~~narrow at the bottom thereof~~ smaller than a width of said first trenches; and

a word line connected to said memory cells, buried in said second trenches and extending along the gate width direction.

2. (currently amended) The semiconductor ~~device~~ memory of claim 1, wherein each of said second trenches is capable of reducing parasitic capacitance

between said floating electrodes of said memory cells adjacent to each other along the gate width direction.

3. (currently amended) The semiconductor ~~device~~ memory of claim 1, wherein each of said second trenches is in the shape of V.

4. (currently amended) [[The]] A semiconductor ~~device of claim 1~~ memory, comprising:

a memory cell array constituted by memory cells, each memory cell having a floating electrode, the memory cells being arranged in a matrix on a semiconductor substrate;

a plurality of first trenches formed in said semiconductor substrate, each first trench being formed between said memory cells adjacent to each other along a gate width direction;

a plurality of isolating fillers filled in said first trenches;

a plurality of second trenches formed in said isolating fillers, each said second trench being formed between said floating electrodes of adjacent ones of said memory cells along the gate width direction, and ~~wherein~~ said second trenches being [[is]] in the shape of an inverted trapezoid; and

a word line connected to said memory cells, buried in said second trenches and extending along the gate width direction.

5. (currently amended) [[The]] A semiconductor ~~device of claim 1~~ memory, comprising:

a memory cell array constituted by memory cells, each memory cell having a floating electrode, the memory cells being arranged in a matrix on a semiconductor substrate;

a plurality of first trenches formed in said semiconductor substrate, each first trench being formed between adjacent ones of said memory cells along a gate width direction;

a plurality of isolating fillers filled in said first trenches;

a plurality of second trenches formed in said isolating fillers, each second trench being formed between said floating electrodes of adjacent ones of said memory cells along the gate width direction, and ~~wherein~~ said second trenches being [[is]] in the shape of a U; and

a word line connected to said memory cells, buried in said second trenches and extending along the gate width direction.

6. (canceled)

7. (currently amended) The semiconductor ~~device~~ memory of claim [[6]] 4, wherein said word line is buried in said second trenches via ~~an insulating film, said insulating film and said~~ a gate insulating film ~~being on the same insulating layer~~.

8. (currently amended) The semiconductor ~~device~~ memory of claim [[1]]7, wherein said gate insulating film includes at least a silicon nitride film.

9. (currently amended) The semiconductor ~~device~~ memory of claim [[1]] 4, wherein a ratio of a top diameter to a bottom diameter of said second trench is ~~large compared with~~ greater than a ratio of ~~those~~ a top diameter to a bottom diameter of said first trench.

10. (currently amended) The semiconductor ~~device~~ memory of claim [[1]] 4, wherein each of said second trenches is shallower than said first trenches and extends below a surface of said semiconductor substrate.

11. (currently amended) The semiconductor ~~device~~ memory of claim [[1]] 4, wherein said ~~non-volatile~~ memory is at least one of a NAND [[or]] and NOR type electrically erasable programmable read only memory.

12. (currently amended) A method of manufacturing a semiconductor ~~device including a non-volatile~~ memory, the method comprising:

making [[an]] element isolating regions by forming a plurality of first trenches in a semiconductor substrate, each said first trench being made between adjacent ones of memory cell forming regions ~~adjacent to each other~~ along a gate width direction[[,]];

~~and by~~ filling said plurality of first trenches with [[an]] a plurality of isolating fillers;

making a plurality of floating gate electrodes on said semiconductor substrate at said memory cell forming regions, said floating gate electrodes having a predetermined gate width;

making a plurality of second trenches in said isolating fillers filled in said first trenches, each second trench being made [[and]] between adjacent ones of the floating electrodes ~~adjacent to each other~~ along [[a]] the gate width direction, a maximum width of said second trenches being ~~narrow at bottoms thereof~~ smaller than a width of said first trenches; and

forming a word line in said second trenches, said word line extending along the gate width direction.

13. (currently amended) The method of claim 12, wherein each of said second trenches is formed in the shape of V.

14. (currently amended) [[The]] A method of manufacturing a semiconductor memory ~~claim 12~~, comprising:

making element isolating regions by forming a plurality of first trenches in a semiconductor substrate, each first trench being made between adjacent ones of memory cell forming regions along a gate width direction;

filling said plurality of first trenches with a plurality of isolating fillers;

making a plurality of floating gate electrodes on said semiconductor substrate at said memory cell forming regions, said floating gate electrodes having a predetermined gate width;

making a plurality of second trenches in said isolating fillers filled in said first trenches, each second trench being made between adjacent ones of said floating

electrodes along the gate width direction, ~~wherein~~ said second trenches being ~~is formed~~ in the shape of an inverted trapezoid; and

forming a word line in said second trenches, said word line extending along the gate width direction.

15. (currently amended) [[The]] A method of manufacturing a semiconductor memory ~~claim 12~~, comprising:

making element isolating regions by forming a plurality of first trenches in a semiconductor substrate, each first trench being made between adjacent ones of a plurality of memory cell forming regions along a gate width direction;

filling said plurality of first trenches with a plurality of isolating fillers;

making a plurality of floating gate electrodes on said semiconductor substrate at said memory cell forming regions, said floating gate electrodes having a predetermined gate width;

making a plurality of second trenches in said isolating fillers filled in said first trenches, each second trench being made between adjacent ones of the floating electrodes along the gate width direction, ~~wherein~~ said second trench being ~~is formed~~ in the shape of a U; and

forming a word line in said second trenches, said word line extending along the gate width direction.

16. (currently amended) The method of claim [[12]] 14, wherein said second trenches are [[is]] in self-alignment to said floating electrodes.

17. (currently amended) A method of manufacturing a semiconductor ~~device including a non-volatile~~ memory, the method comprising:

making floating gate electrodes on a semiconductor substrate at memory cell forming regions, said floating gate electrodes having a predetermined gate width;

making a plurality of first trenches in said semiconductor substrate, each said first trench being made [[and]] between adjacent ones of said floating gate electrodes ~~adjacent to each other~~ along a gate width direction, said first trenches being in self-alignment to said floating gate electrodes;

making [[an]] element isolating regions by filling [[an]] isolating fillers in said first trenches;

making a side wall spacer on a surface of each of said isolating fillers in a side wall of said floating gate electrodes, said side wall spacer being in self-alignment to said floating gate electrodes;

making a plurality of second trenches in said isolating fillers filled in said first trenches using said side wall spacer as a mask, a maximum width of said second trenches being smaller than a width of said first trenches; and

forming a word line in said second trenches, said word line extending along the gate width direction.

18. (new) The semiconductor memory of claim 4, wherein said second trenches has a second gate insulating film on inner surfaces thereof.

19. (new) The method of claim 14, wherein each of said second trenches has a second gate insulating film on inner surfaces thereof.

20. (new) The method of claim 17, wherein each of said second trenches has a second gate insulating film on inner surfaces thereof.